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Attorney Docket No. 20040144.ORI

Client Docket No. CFP00353

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re App	:	Herng-Jer Lee et al.	:	Examiner James C. Kerveros
Serial No.	:	10/827,507	:	Art Unit 2138
Filed	:	April 19, 2004	:	Confirmation No. 3480
For	:	Method of Scan Chain Reordering for Lowering VLSI Power Consumption		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I CERTIFY THAT THIS PAPER IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE AS FIRST CLASS MAIL WITH SUFFICIENT POSTAGE AND IS ADDRESSED TO: COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450, ON SEPREMBER 18, 2006 (37 C.F.R. 1.8a).

PETITION FOR EXTENSION OF TIME

Sir:

Applicant hereby petitions the Commissioner for a two-month extension of time to respond to the Official Action mailed April 17, 2006, in the above-captioned patent application.

A check in the amount of $225.00 is enclosed to cover the extension fee.

The Commissioner is hereby authorized to charge any additional fees under 37 CFR 1.16 and 1.17 which may be required by this paper to Deposit Account No. 08-1265.

Respectfully submitted,

Herng-Jer Lee et al.

Dated: September 18, 2006.

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